Features

- ESD/Surge protect for 2 differential line pairs (4 lines) with bi-direction
- Provide transient protection for the protected differential line pair to

  IEC 61000-4-2 (ESD) ±30kV (air/contact)

  IEC 61000-4-4 (EFT) 80A (5/50ns)

  IEC 61000-4-5 (Lightning) 18A (8/20μs)
- For low operating voltage applications: 3.3V maximum
- Low capacitance : 0.9pF typical
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- 10/100/1000 ethernet
- xDSL line protection
- WAN/LAN device
- Notebook and PC computers

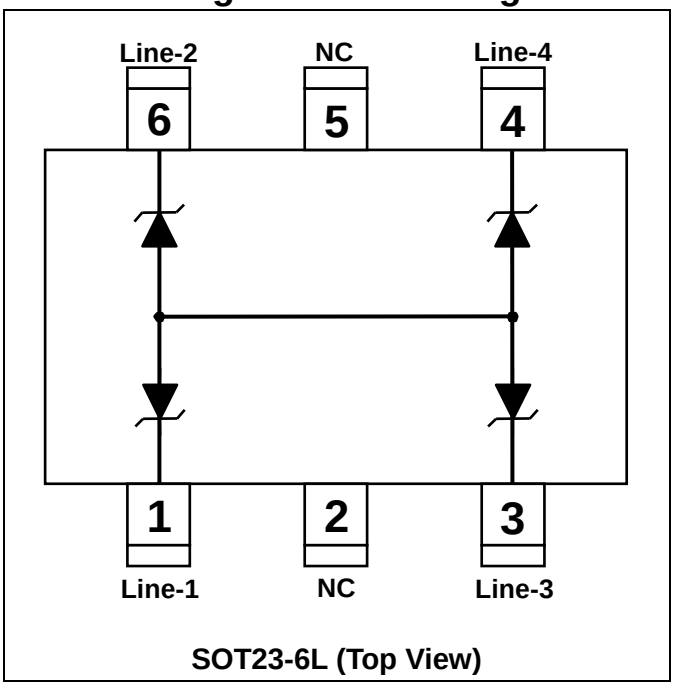
Description

AZ1603-02S is a design which includes bi-directional surge rated clamping cells to protect two differential high speed data-line pairs in an electronic system. The AZ1603-02S has been specifically designed to protect the differential line pairs from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

During transient conditions, the proprietary clamping cells provide low clamping voltage to minimize the stress on the protected components.

AZ1603-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



SOT23-6L (Top View)

Specifications

Absolute Maximum Ratings (T_A= 25°C, unless otherwise specified)			
Parameter	**Symbol**	**Rating**	**Unit**
Peak Pulse Current (tp=8/20μs)	I_{PP} (Note 1)	18	A
Operating Voltage	V_{DC}	±3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

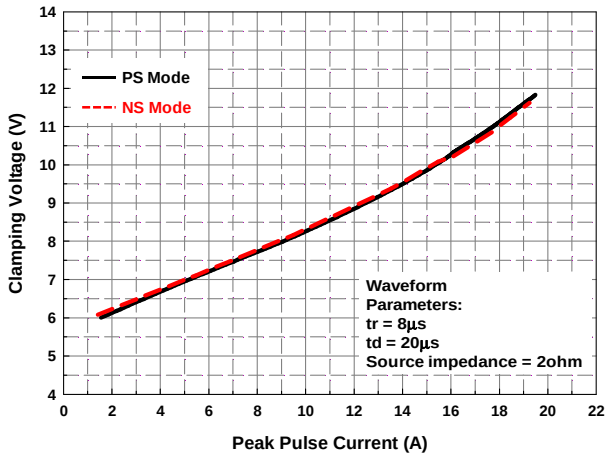
Electrical Characteristics						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C.	-3.3		3.3	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = ±3.3V, T=25 °C, each differential line pair.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, each differential line pair.	4		7	V
ESD Clamping Voltage (Note 2)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, contact mode, each differential line pair.		10		V
ESD Dynamic Turn on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, T=25 °C, contact mode, each differential line pair.		0.28		Ω
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP}=5A, tp=8/20μs, T=25 °C, each differential line pair.		7		V
		I_{PP}=18A, tp=8/20μs, T=25 °C, each differential line pair.		11		V
Input Capacitance	C_{IN}	V_{IN} =0V, f =1MHz, T=25 °C, each differential line pair.		0.9	1.2	pF

Note 1: The Peak Pulse Current measured conditions: t_p = 8/20μs, 2Ω source impedance.

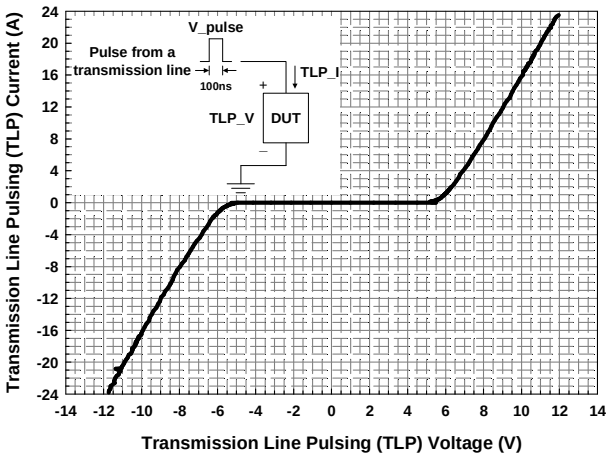
Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

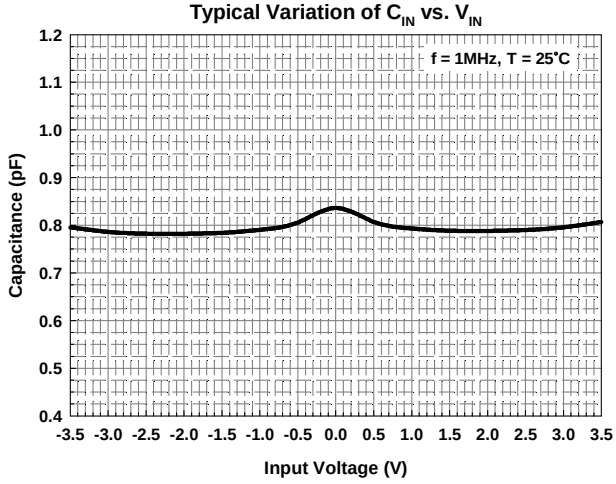
Reverse Clamping Voltage vs. Peak Pulse Current



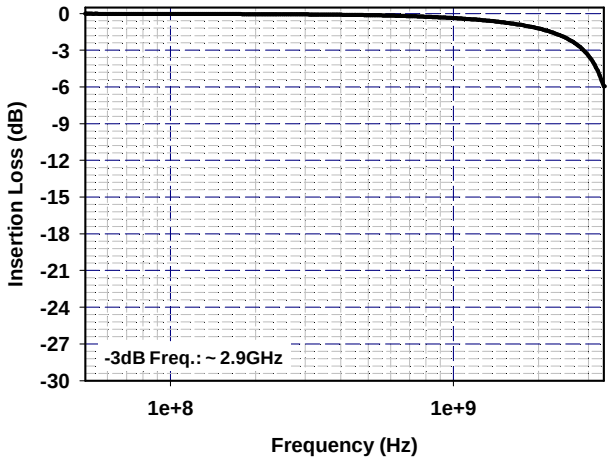
Transmission Line Pulsing (TLP) Measurement



Typical Variation of C_{IN} vs. V_{IN}



Insertion Loss S21 (each differential line pair)



Applications Information

The AZ1603-02S is designed to protect 2 differential line pairs (4 lines) against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference. It provides bi-directional protection.

Fig. 1 shows a typical Gigabit Ethernet protection circuit with AZ1603-02S for lines-to-lines protection. Four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4 and pin6) of AZ1603-02S. Pin2 and pin5 of AZ1603-02S are not connected.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ1603-02S.
- Place the AZ1603-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path should be kept as short as possible.
- NEVER route critical signals near board edges and near the lines which the ESD transience easily injects to.

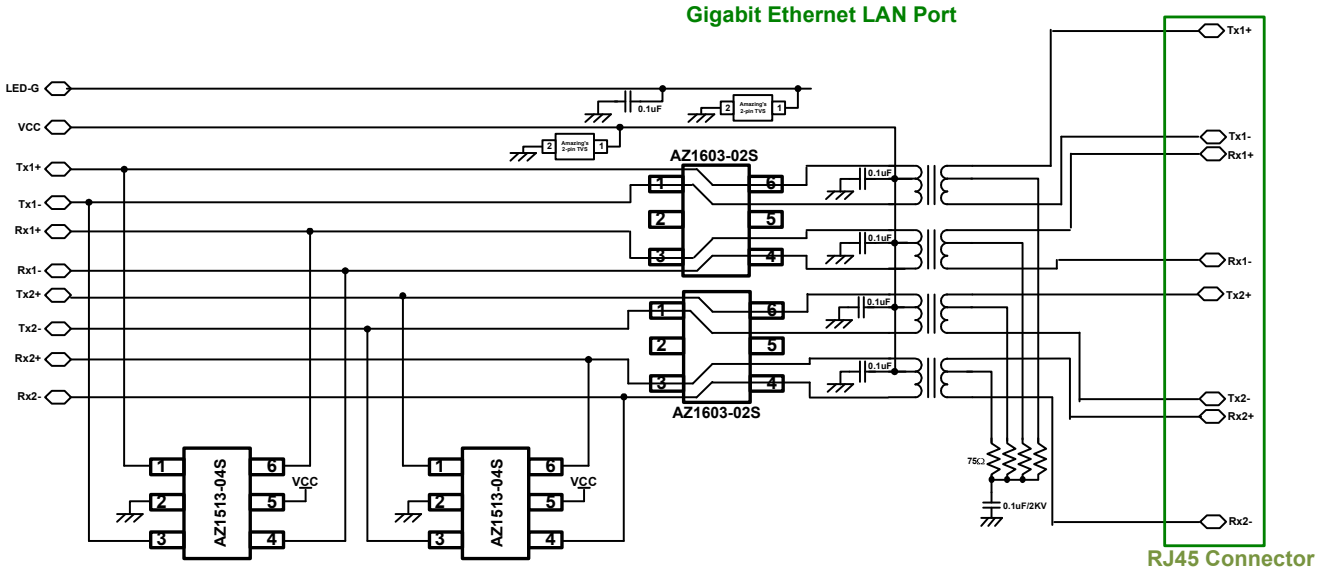


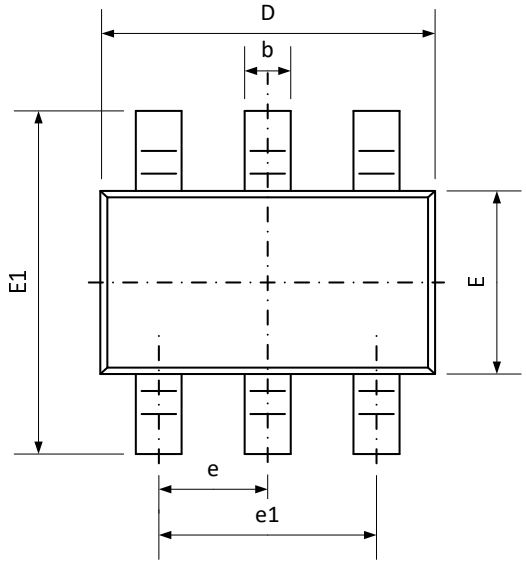
Fig. 1 Gigabit Ethernet surge protection circuit with AZ1603-02S.

Mechanical Details

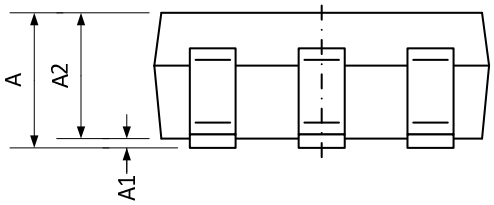
SOT23-6L

Package Diagrams

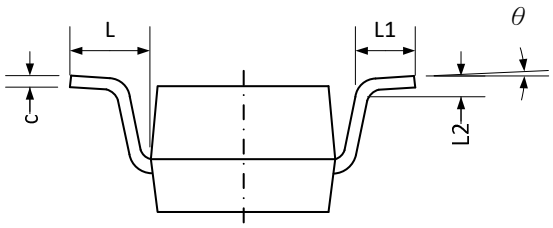
TOP VIEW



SIDE VIEW



END VIEW



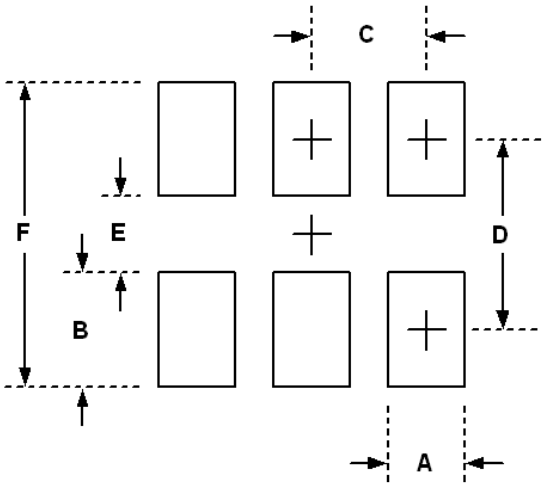
Package Dimensions

Symbol	Millimeters	
	Min.	Max.
A	-	1.25
A1	0.00	0.10
A2	0.90	1.20
b	0.30	0.50
c	0.08	0.21
D	2.72	3.12
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
e1	1.90 BSC	
L1	0.30	0.60
L	0.70 REF	
L2	0.25 BSC	
θ	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters.

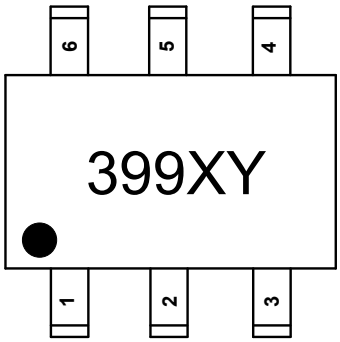
Land Layout



Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



399 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ1603-02S.R7G (Green Part)	399XY

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ1603-02S.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

Revision History

Revision	Modification Description
Revision 2019/10/15	Formal Release.